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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,829	TSUKIHASHI, AKIRA	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This final office action is in response to amendments filed on 2/22/05.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-10, 17-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sartore et al., US Patent no. 6,839,778 [Sartore].

Regarding claim 1, Sartore discloses a circuit comprising:

a power source determination circuit for determining a type of power source [column 3, lines 19-23];

a power feeding switching circuit [control block] for setting an amount of current to be supplied to a processing circuit conducting processing for data transfer, based on a result of determination made by the power source determination circuit [column 2, lines 1-7 and column 3, lines 19-22]; and

a clock switching circuit [control block] for setting operation clocks for the processing circuit according to a result of determination made by the power source determination circuit [column 2, lines 1-7 and column 3, lines 19-22 and 49-51], wherein

a data transfer rate is set according to the type of power source [column 3, lines 19-22 and 49-51]; and

wherein the interface circuit operates as an upper version USB interface circuit [480 Mbs USB 2.0] when an external power source is connected [column 3, lines 19-22 and 49-51], and operates as a lower version USB interface circuit [12 Mbs] when no external power source is connected [column 3, lines 19-22 and 49-51].

Regarding claim 2, Sartore further discloses that the power source determination circuit determines whether an external power source is connected, and when is determined that an external power source is connected, the power feeding switching circuit increases the amount of current and the clock switching circuit sets a faster clock, so that high speed data transfer [480 Mbs] is carried out, and when is determined that no external power source is connected, the power feeding switching circuit causes to reduce the amount of current and the clock switching circuit sets a slower clock, so that slow speed data transfer [12 Mbs] is carried out [column 3, lines 19-22 and 49-51].

Regarding claims 3 and 4, Sartore, as described above, discloses that the circuit operates as a 480 Mbs USB 2.0 circuit when an external power source is connected and as a 12 Mbs USB circuit when no external power source is connected. Sartore does not specifically state that the 12 Mbs is a USB 1.1 version. However, it is well known in the art that USB 1.1 devices operate with a maximum speed of 12 Mbs. Therefore the circuit is inherently operating under USB 1.1 when an external power source is not connected.

Regarding claim 7, Sartore discloses an interface circuit for USB data transfer comprising:

a power source determination means for determining a type of power source [column 3, lines 19-23];

a power switching means [control block] for switching between a proper amount of current to be supplied to a processing circuit conducting processing for data transfer, based on a result of determination made by the power source determination means [column 2, lines 1-7 and column 3, lines 19-22]; and

a clock switching means [control block] for setting operation clocks for the processing circuit according to a result of determination made by the power determination means [column 2, lines 1-7 and column 3, lines 19-22 and 49-51], wherein

a data transfer rate is set according to the type of power source [column 3, lines 19-22 and 49-51].

wherein the interface circuit operates as an upper version USB interface circuit [480 Mbs USB 2.0] when an external power source is connected [column 3, lines 19-22 and 49-51], and operates as a lower version USB interface circuit [12 Mbs] when no external power source is connected [column 3, lines 19-22 and 49-51].

Regarding claim 8, Sartore further discloses that the power source determination means determines whether an external power source is connected, and when it is determined that an external power source is connected, the power switching means increases the amount of current and the clock switching means sets a faster clock, so that high speed data transfer [480 Mbs] is carried out, and when it is determined that no external power source is connected, the power switching means causes to reduce the amount of current and the clock switching means sets a

slower clock, so that slow speed data transfer [12 Mbs] is carried out [column 3, lines 19-22 and 49-51].

Regarding claims 9 and 10, Sartore, as described above, discloses that the circuit operates as a 480 Mbs USB 2.0 circuit when an external power source is connected and as a 12 Mbs USB circuit when no external power source is connected. Sartore does not specifically state that the 12 Mbs is a USB 1.1 version. However, it is well known in the art that USB 1.1 devices operate with a maximum speed of 12 Mbs. Therefore the circuit is inherently operating under USB 1.1 when an external power source is not connected.

Regarding claims 17 and 20, Sartore discloses discloses a method of determining a rate of transfer comprising:

determining a type of power source [column 3, lines 19-23];

setting an amount of current to be supplied to a processing circuit conducting processing for data transfer, based on a result of the determination of the type of power source [column 2, lines 1-7 and column 3, lines 19-22]; and

setting operation clocks for the processing circuit according to the determination of the type of power source [column 2, lines 1-7 and column 3, lines 19-22 and 49-51], wherein

a data transfer rate is set according to the type of power source [column 3, lines 19-22 and 49-51].

further comprising operating as a USB ver. 2.0 interface circuit when an external power source is connected [column 3, lines 19-22 and 49-51], and operating as a USB ver. 1.1 interface [12 Mbs] circuit when no external power source is connected [column 3, lines 19-22 and 49-51].

Sartore discloses that the circuit operates as a 480 Mbs USB 2.0 circuit when an external power source is connected and as a 12 Mbs USB circuit when no external power source is connected. Sartore does not specifically state that the 12 Mbs is a USB 1.1 version. However, it is well known in the art that USB 1.1 devices operate with a maximum speed of 12 Mbs. Therefore the circuit is inherently operating under USB 1.1 when an external power source is not connected.

Regarding claim 18, Sartore further discloses determining whether an external power source is connected, and when it is determined that an external power source is connected, increasing the amount of current and setting a faster clock, so that high speed data transfer [480 Mbs] is carried out, and when it is determined that no external power source is connected, reducing the amount of current and setting a slower clock, so that slow speed data transfer [12 Mbs] is carried out [column 3, line 66 – column 4, line 6 and column 7, lines 44-58].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sartore et al., US Patent no. 6,839,778 [Sartore].

Regarding claims 5 and 11, Sartore does not specifically state that the circuit is a disk drive. Sartore does state that the circuit may be any type of computer peripheral device [column 1, lines 60-64]. USB disk drives are well known in the art and it would have been obvious to one of ordinary skill in the art to apply the teachings of Sartore in a well known USB disk drive.

Regarding claims 6 and 12, Sartore does not explicitly disclose that the peripheral sends the computer data concerning a data transfer rate at a time of resetting the interface circuit. However, it would have been obvious to one of ordinary skill in the art that some sort of indication regarding the transfer rate would be sent to the computer to ensure that the peripheral and the computer may successfully communicate data.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sartore et al., US Patent no. 6,839,778 [Sartore], in view of, Tomlinson et al., US Patent no. 6,735,706 [Tomlinson][1].

Regarding claims 13 and 14, Sartore discloses a circuit that is able to operate at a plurality of power consuming modes. It is inherent in the teachings of Sartore that some sort of multiple voltage power supply must be included in the circuit to provide power to the circuit components. Sartore does not explicitly disclose a power supply comprising a DC/DC converter. However, as shown by Tomlinson, it is well known in the art to use to DC/DC converters in power supplies with multiple output voltages [column 4, lines 4-10]. Therefore it would have been obvious to one of ordinary skill in the art to use a well known DC/DC converter to allow for multiple output voltages in the selectable output voltage power supply.

[1] included in previous office action

Regarding claims 15 and 16, Tomlinson discloses that the power supply may output voltage values of 2.5V, 3.3V and 5V [column 4, lines 11-12].

Response to Arguments

Applicant's arguments with respect to claims 1-18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

REHANA PERVEEN
PRIMARY EXAMINER

Paul Yanchus
May 12, 2005